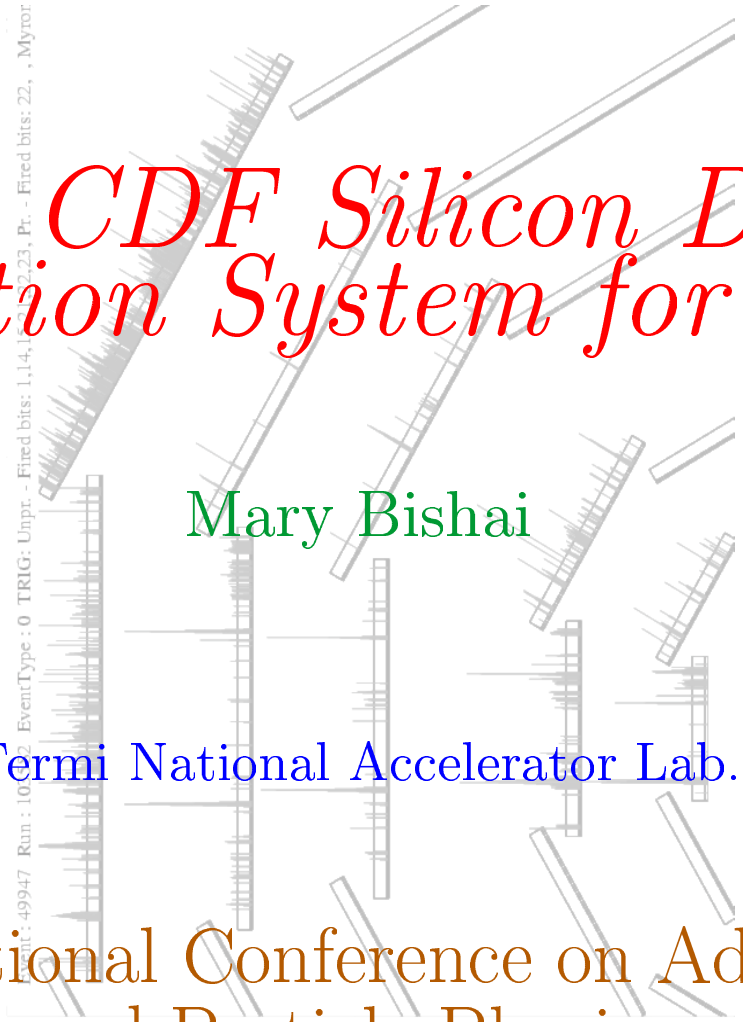

The CDF Silicon Data Acquisition System for Run II

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Fermi National Accelerator Lab.

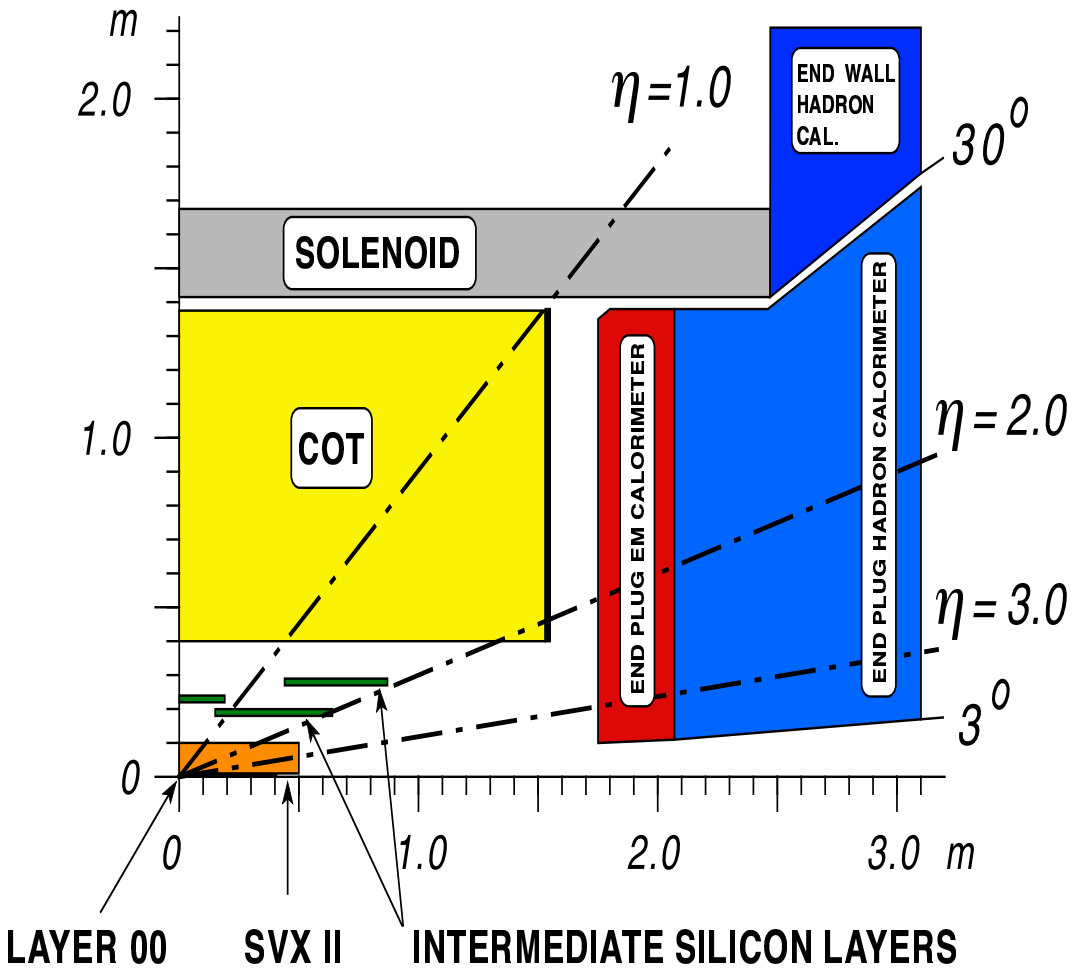
International Conference on Advanced Technology and Particle Physics , Como Oct 15-19$^{\text{th}}$ 2001

CDF II Si

SVXII: 3 barrels (90cm) with 5 layers of double sided silicon. 3 90^o and 2 small angle stereo layers. *60-140 μm pitch*

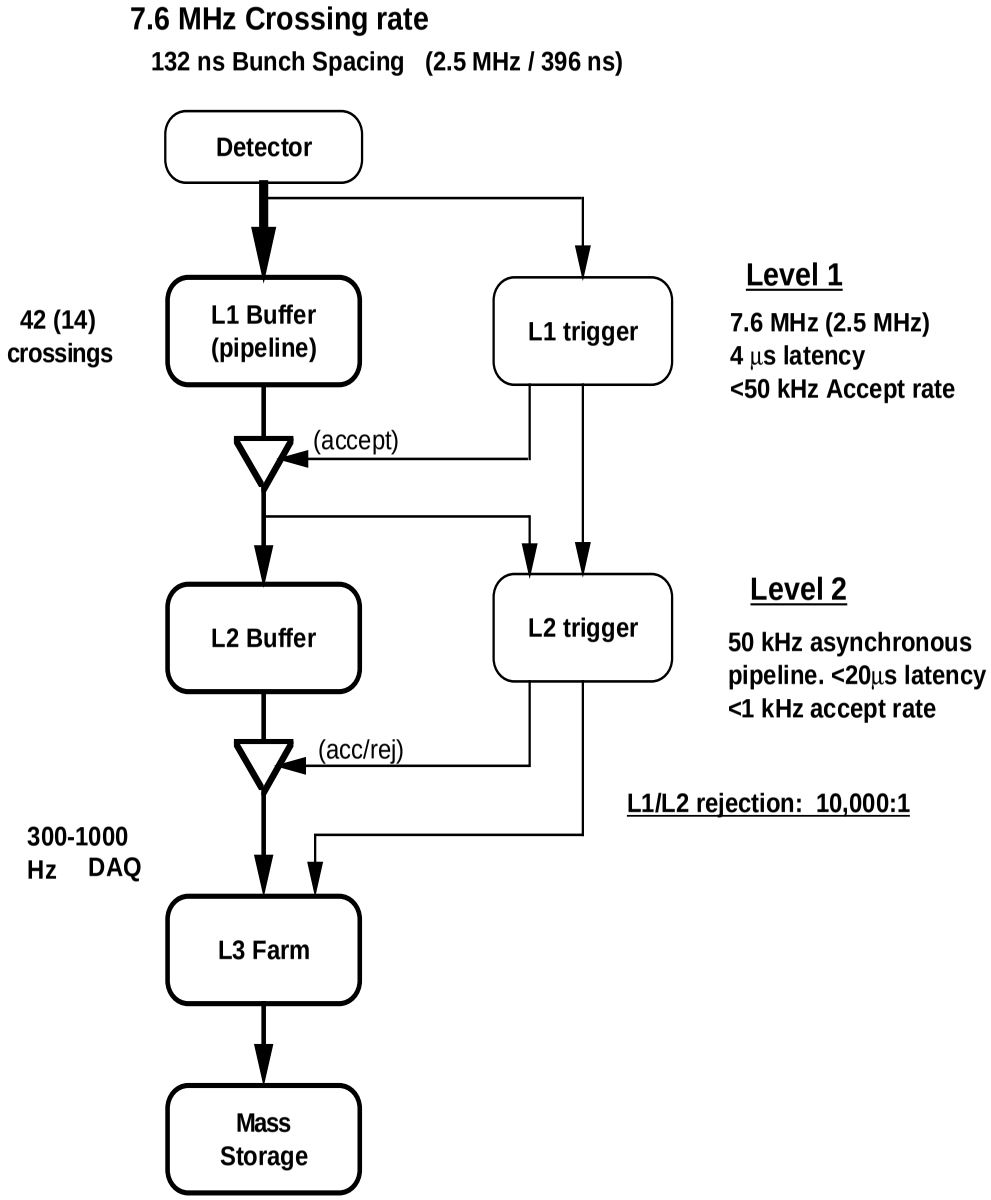
ISL: 1 layer of Si at $|\eta| < 1$, 2 layers at $1.0 < |\eta| < 2$. *112 μm pitch*

L00: Single sided Si layer on Be beam pipe. *50 μm pitch*



Over 700,000 readout channels.

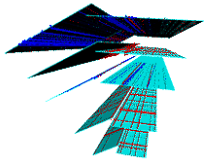
Si DAQ Specifications



L1 latency: Pipeline depth = L1 processing time $\sim 5\mu$secs. *The SVXII detector is readout on L1 Accept.*

L2 processing time: The Silicon Vertex Trigger is in L2 $\Rightarrow$ *full readout of the Silicon system has to take place in* $\sim 10\mu$*secs +* $\sim 10\mu$*secs SVT processing time = L2 latency.*

Overview of the Si DAQ



Daq Components:

The SVX3D chip: Analog front end amplifies signal from 128 Si strips, stores charge on a pipeline of 46 capacitors (cells). Independent back end digitizes and transmits 8 bits of data and a data clock.

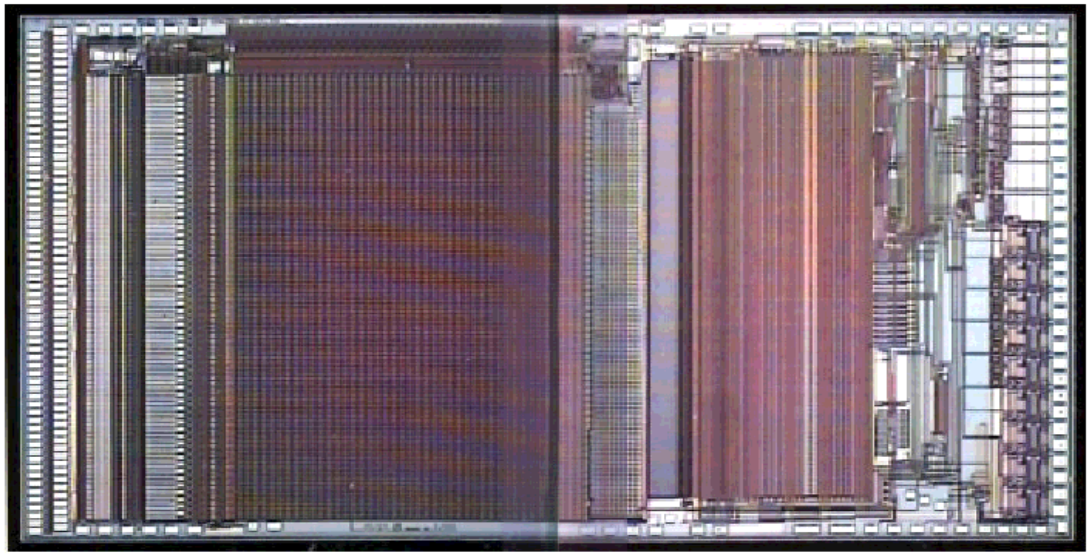
Compact Port Card (CPC): Transmits control signals from DAQ to SVX3D chips. Optically transmits 9 data bits to DAQ front-end.

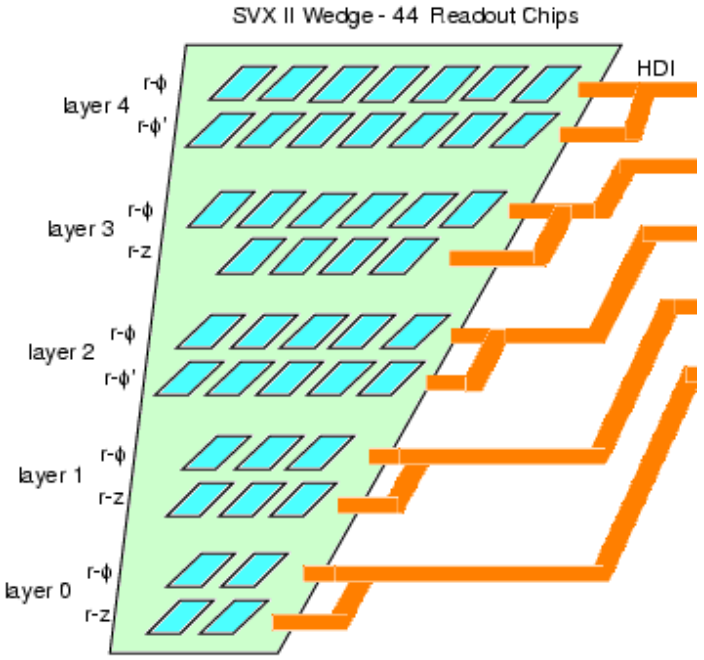
Fiber Interface Board (FIB): Receives optical readout from CPC. Flash RAM used for programming and storing SVX3D control sequences.

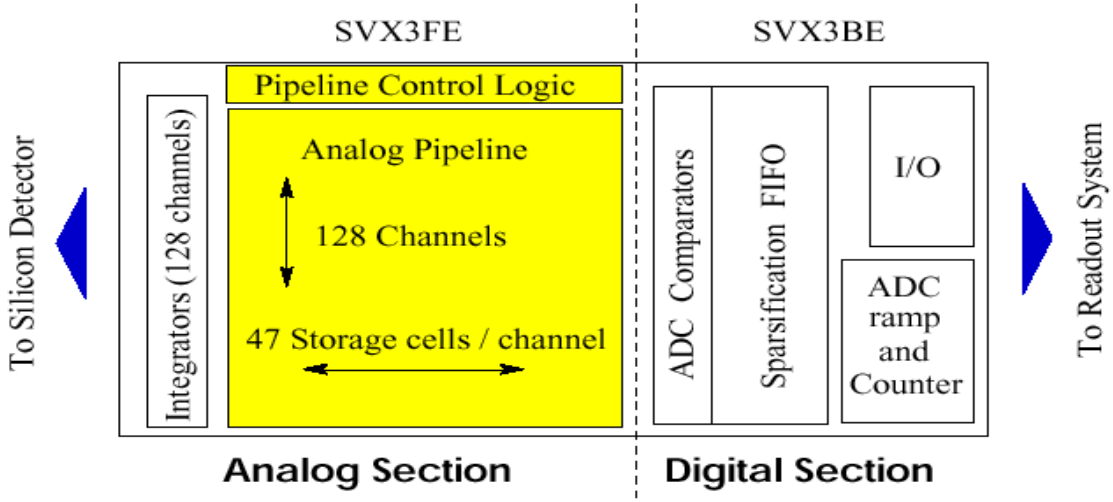
VME Readout Buffer (VRB): Receives data from FIBs and stores in memory buffers to be collated by the CDF Hardware Event Builder (HEVB).

Silicon Readout Controller: Interface between CDF DAQ and Si DAQ systems. Handles intricate timing needed to synchronize Si readout/operation with the rest of CDF. THE BRAIN.

The SVX3D Chip

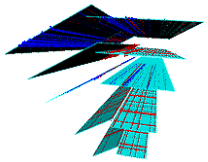






Rad-hard 0.8 μm Honeywell CMOS. Each chip reads out 128 strips.

The SVX3D Chip Features



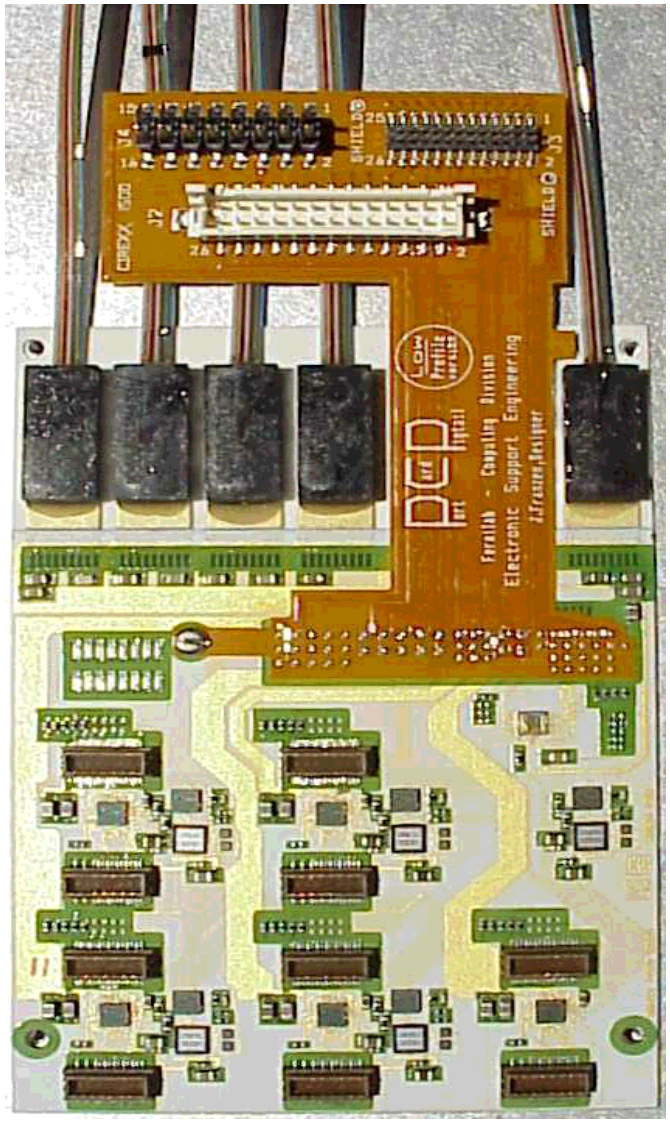
Pipelined: A total of 46 cells. The pipeline depth is 42 cells deep. 1 reference cell/channel is used to eliminate channel-channel pedestal variation. Up to 4 of the pipeline cells can be tagged at by a L1Accept regardless of back-end state for *deadtimeless* operation.

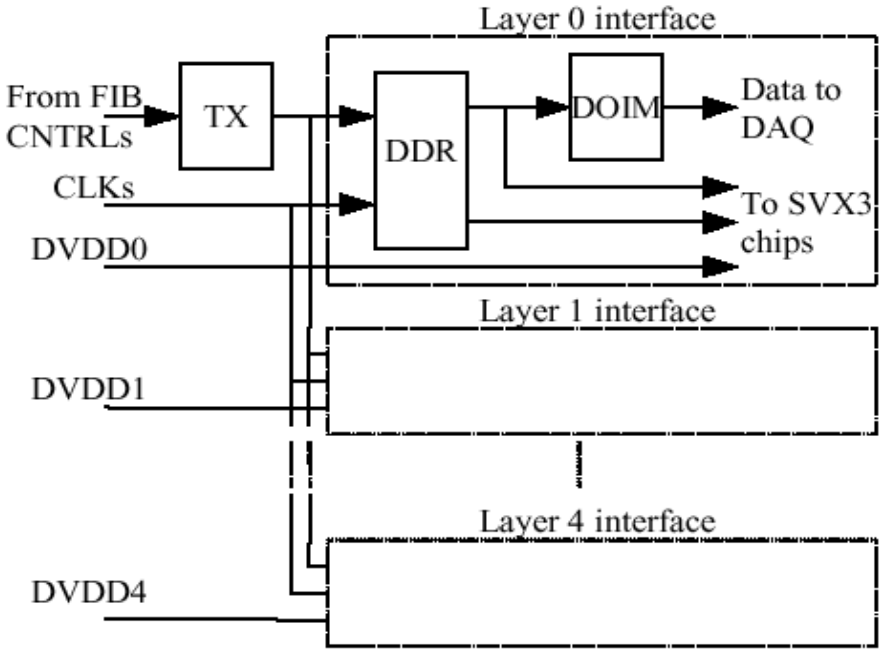
Analog/Digital integrated A digital back-end separate from the analog front end sparsifies and digitizes the analog signal using an 8-bit ADC. *Compact design.*

Dynamic Pedestal Subtraction: By delaying the start of the digitization counter until 30-40 strips have fired, an event by event pedestal subtraction is applied to the data. *Minimizes common mode noise.*

Programmable settings: 197 bits control operation. 128 channel masks, preamp band width settings, ADC ramp settings, ADC bandwidth, polarity settings, sparsification modes. *Allows the same chip to be used with different Si ladders*

The Compact Port Card





Beryllia module that controls, reads out and regulates power for SVX3D chips. Uses fiber optic transmitters. Each CPC readouts out 5 SVXII ladders in a 30 ^{0} wedge = 44 chips (80 ISL chips). 14 cm from the beam. Severe constraints on size, rad-hardness.

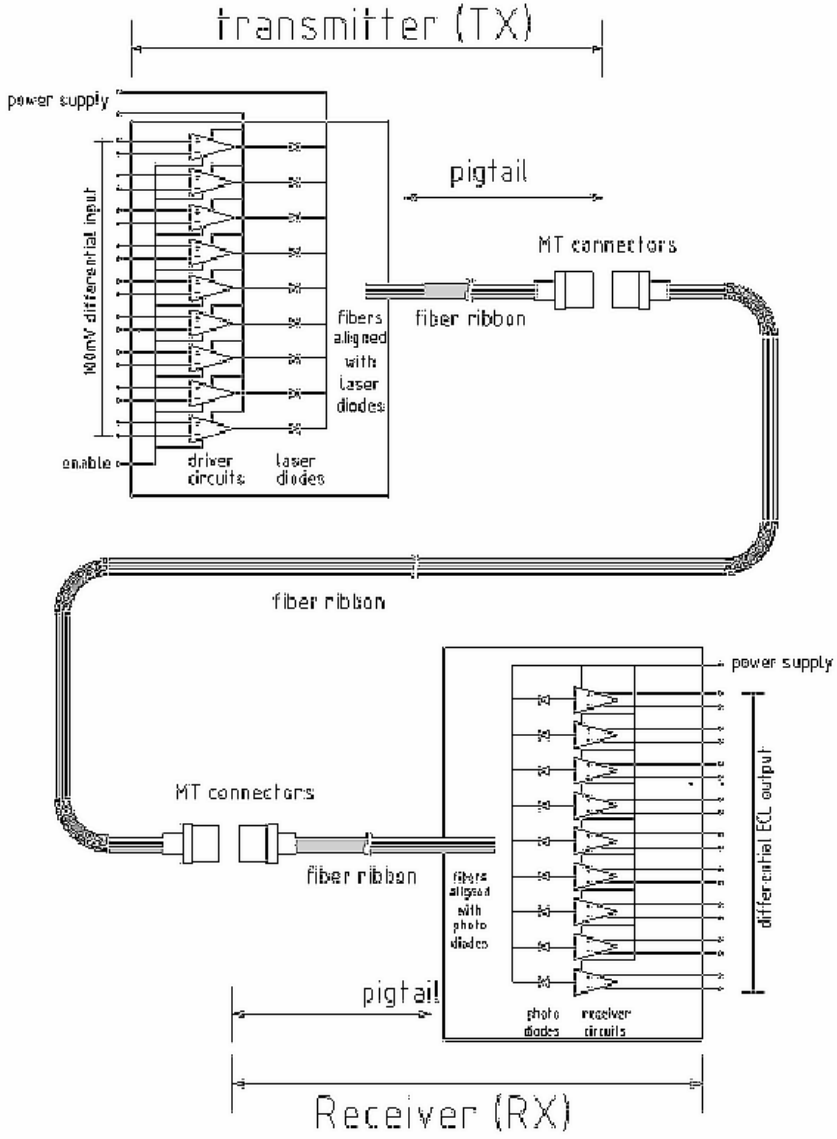
The Compact Port Card Components

Transceiver Chip: Converts low-voltage differential signals (LCDS) from DAQ to single ended CMOS.

Digital Data Receiver (DDR): Decodes 5 bit commands into 10 SVX3D chip CMOS control signals + 4-bit DAC calibration voltages.

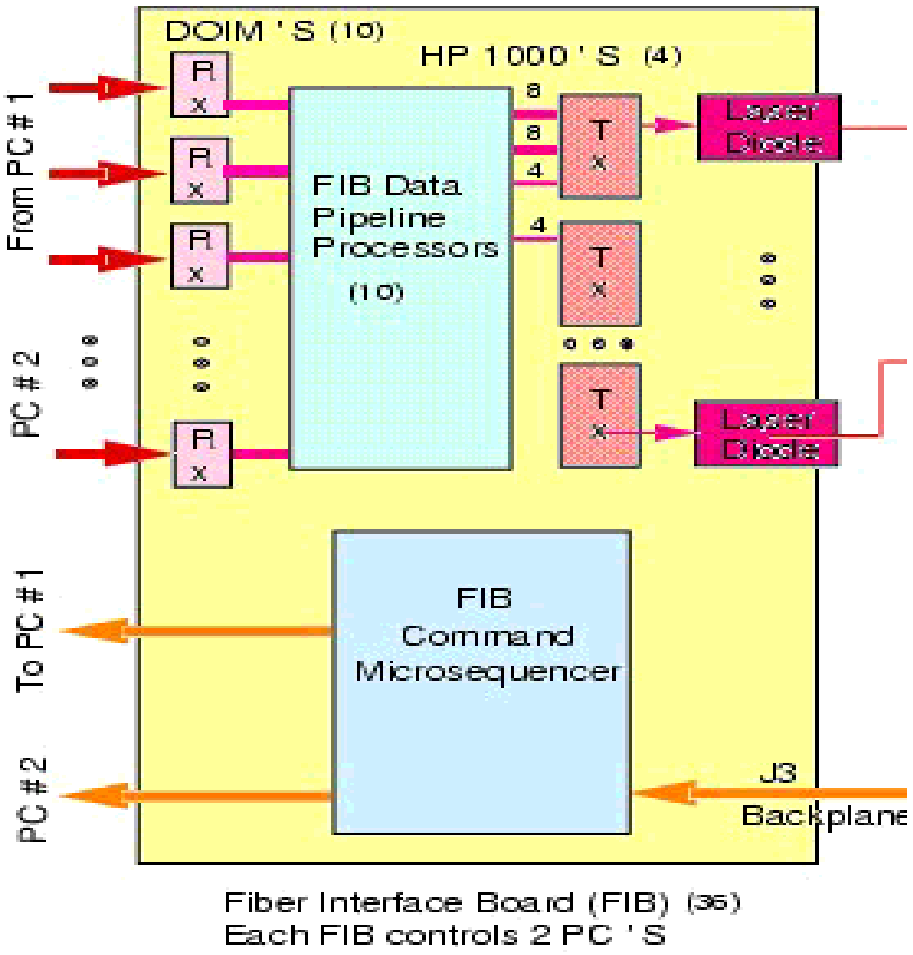
Analog DDR: Regulates chip analog FE voltage (AVDD).

Dense Optical Interface Module: Converts differential 9 bit digital data from chip into optical and transmits to FIB, DAQ FE VME board.



Fiber Interface Board (FIB)

A VMEbus board. Controls the SVX3D chips and transfers data to the L2 data collection buffers (VMEbus Readout Buffers)



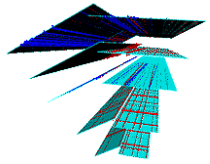
Microsequencer: Converts SRC commands into DDR-encoded SVX3D command sequences.

OFTM: 10 RX-DOIMS on Optical FIB transition Module convert optical data from CPC.

Optical G-Link: Transmits data from 10 input channels via 4 optical G-Links (GHz link) to VRB/SVT.

Flash RAM: lookup table is used to subtract pedestals on a strip by strip basis.

VMEbus Readout Buffer (VRB)



Multiport memory board designed to buffer and filter data for transfer to Level 3 online processors. 10 independent input ports and a common VME output port. Input data rate 50 MBytes/sec/channel. Output data rate 50 MBytes/sec.

Event Buffers: The number of buffers, size and operating modes are programmable. CDF DAQ uses 4 2K read buffers/channel

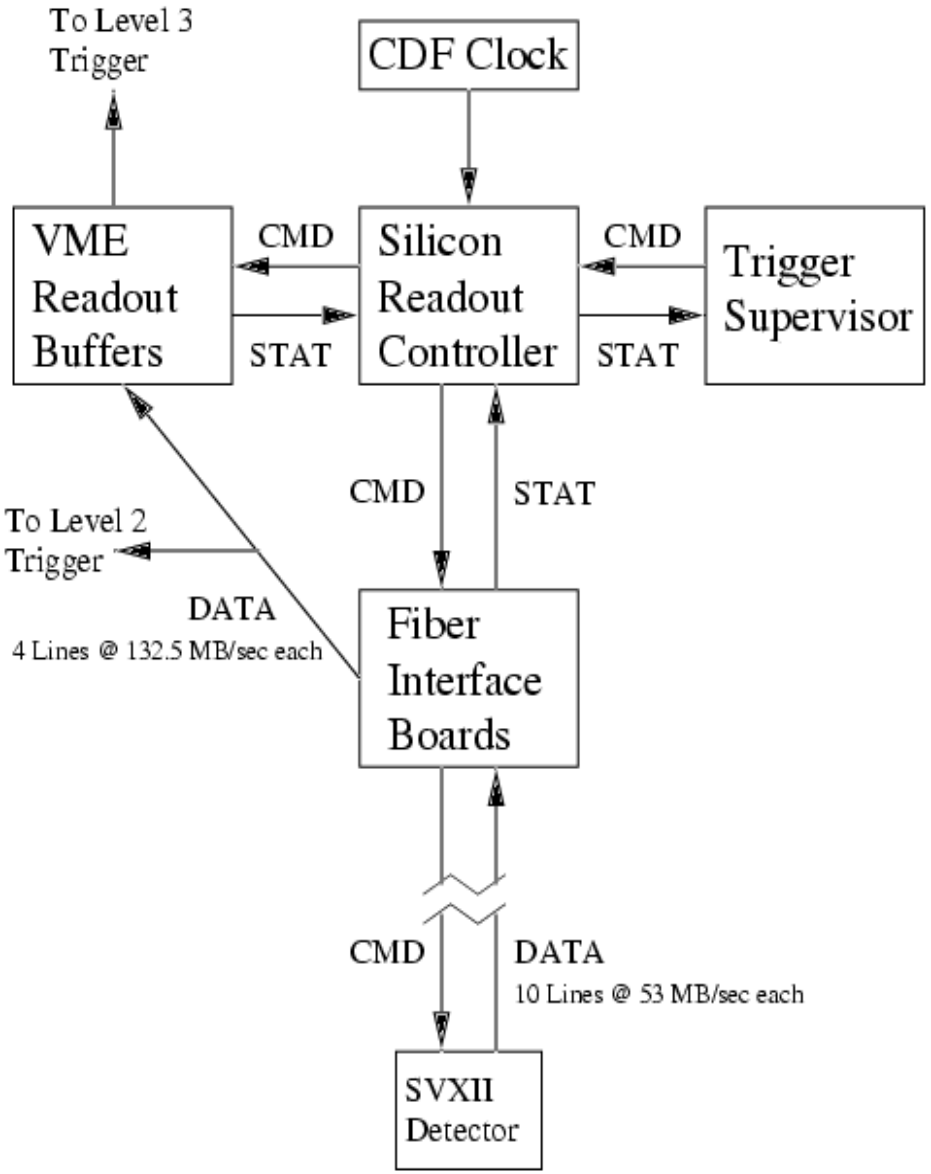
Output Data FIFO: Data is pipelined into a 16KByte output data FIFO.

G-Link receivers: Data from 10 FIB channels is read in over 4 1 Gbps G-Links.

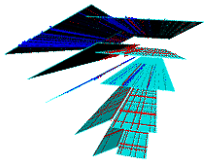
Flash RAM: Pipeline cell ids from each chip are checked for synchronization and compared to the expected pipeline cell received from the SRC. Cross checks bunch crossing numbers received from the SRC with those from each FIB channel. Strip occupancy histograms are stored on board for online monitoring.

Silicon Readout Controller

To control the large data throughput and insure proper deadtimeless operation a special controller is used as an interface between CDF and Si DAQ. The controller board comprises a set of State Machines which change state every 132ns. The Si detector data dominates CDF events ⇒ fast detection of data integrity errors is crucial!



SRC Features



TAXI control: Receives/latches 53 MHz synch clock, RF clock, accelerator bunch crossing structure and TS L1A over a 175 MHz optical TAXI link.

Readout State Machine: On L1A, issues digitize, readout commands to FIBs, buffer numbers, bxing numbers to VRB. Monitors VRB status and throttles CDF TS when buffers are full. *Detects 20 μsec beam gaps and sends preamp resets and PRD2 (pipeline cell release) to FIBs.*

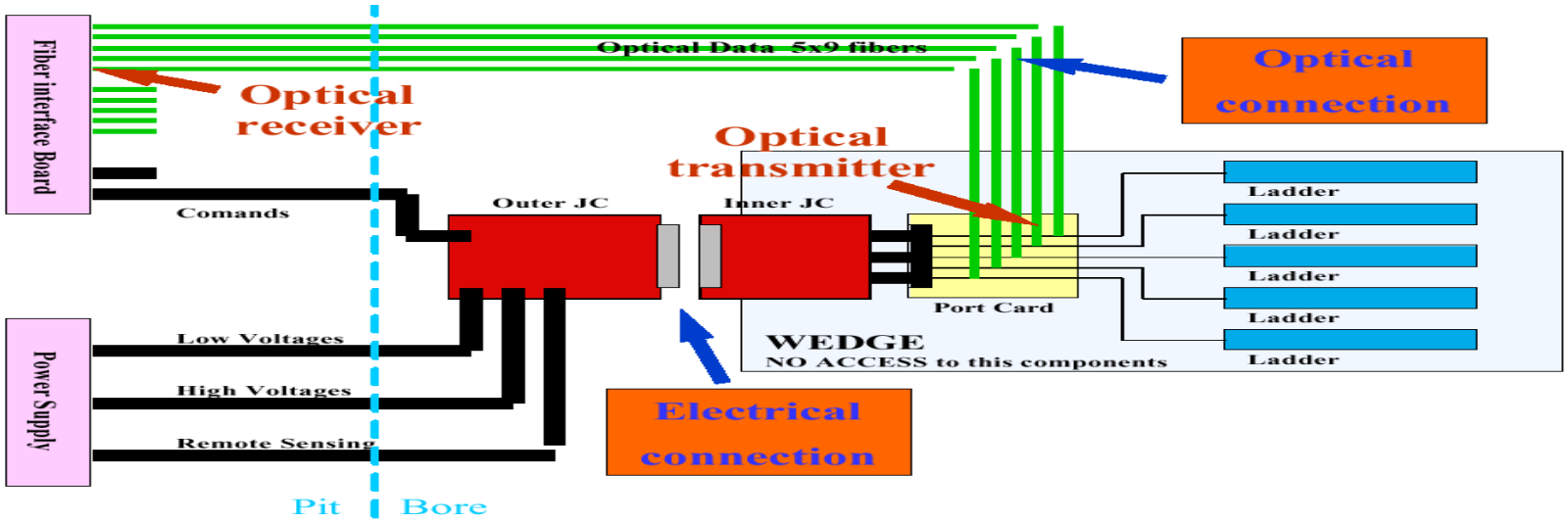
Master Clock: Emulates bunch crossing structure in teststand mode. Processes bunch structure from CDF CLOCK and produces delayed signals.

TS Emulator: Emulates CDF TS in several programmable modes including deadtimeless triggers. *Enables full Si DAQ to operate stand-alone.*

Fib Interface: Synchs pipeline advance clock, L1A, PRD2, FIB commands and sends to Fib Fanouts over G-Links.

Error Logger: Receives/monitors FIB/VRB error reports from fanouts. *SRC halts CDF Run Control upon receiving a fatal FIB/VRB error.*

DAQ Integration with CDF and Si Detector

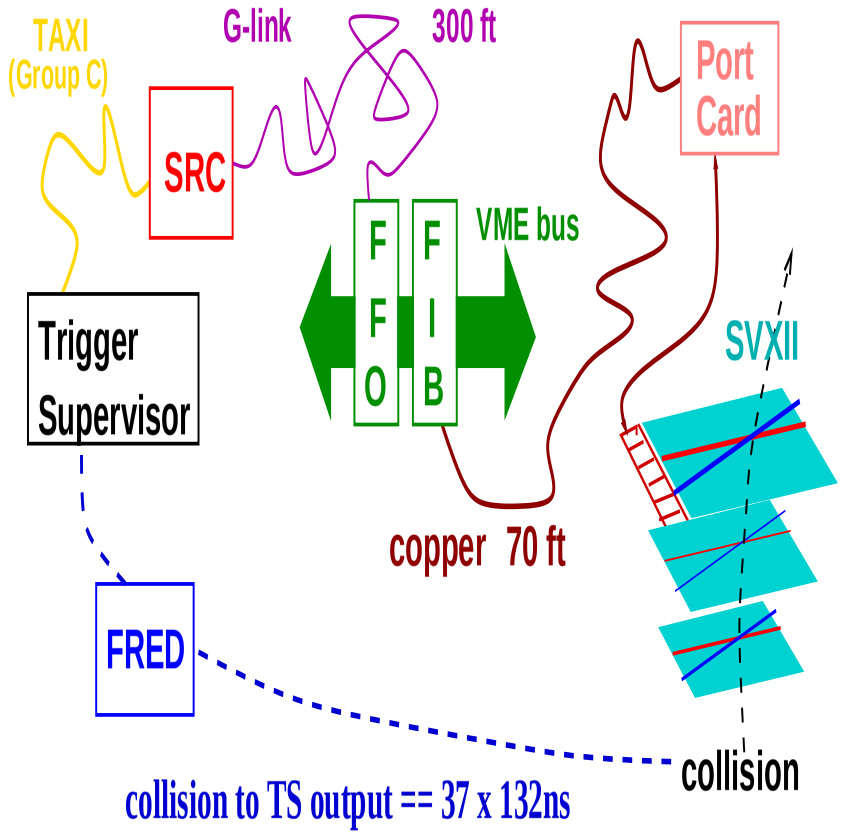


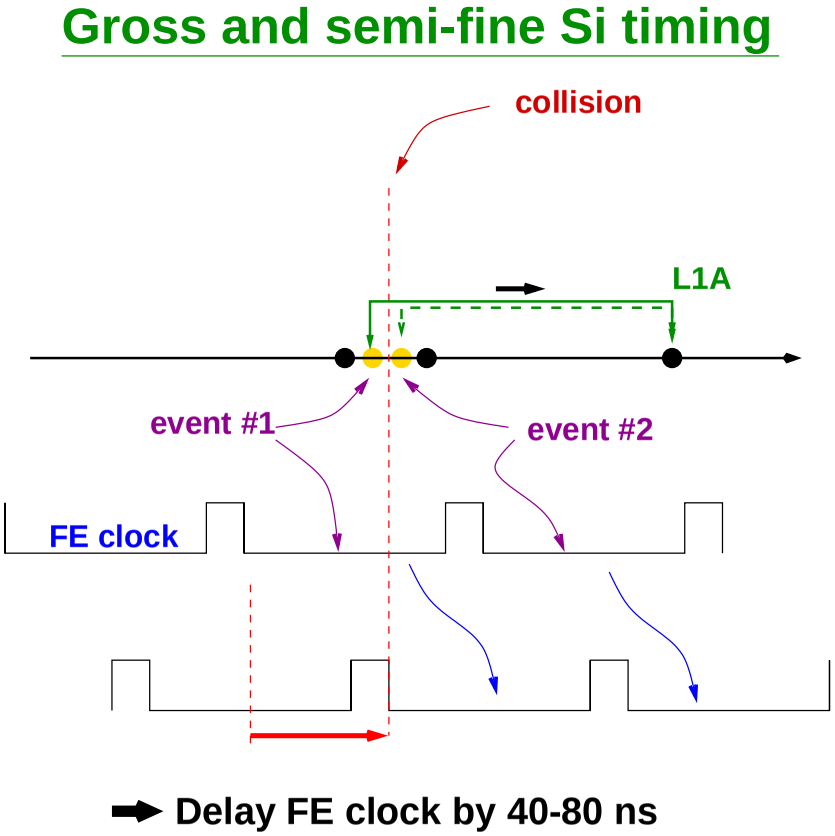
VME Board Integration 20 programmable data emulator boards were installed in the back of the FIB crates emulating data from Si ladders. Tested data throughput, bit error rates, and TS-SRC-FIB-VRB command/data path. *All 148 VME boards were fully integrated and tested with CDF DAQ in the collision hall INDEPENDENT of the Silicon detectors.*

Integration with Silicon 5 fully instrumented Si DAQ test-stands (SRC-FIB-VRB) used during all stages of production: hybrid $\rightarrow$ ladder $\rightarrow$ CPC $\rightarrow$ barrel. *Si detectors tested with full DAQ readout chain.*

Si Commissioning

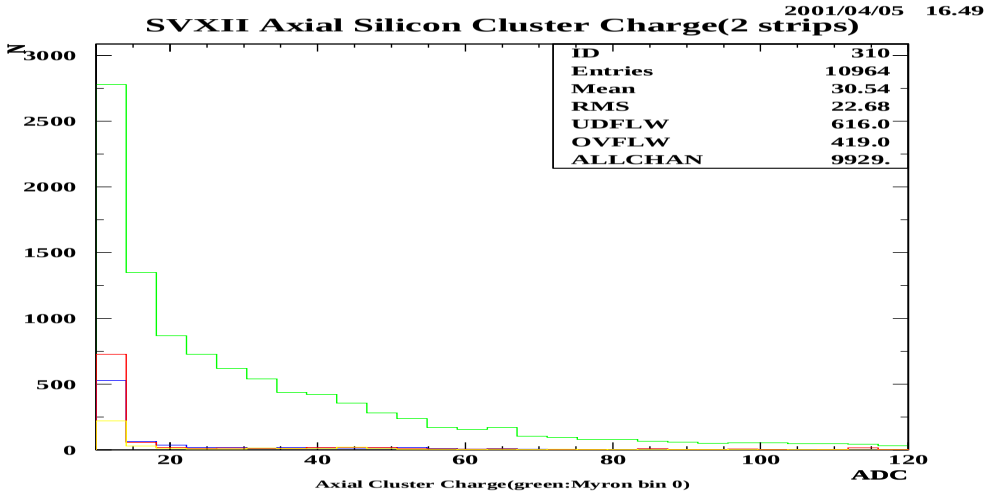
One of the first goals of the engineering and commissioning run was to make sure Si was synchronized with the rest of CDF and the accelerator. The SRC makes this possible:

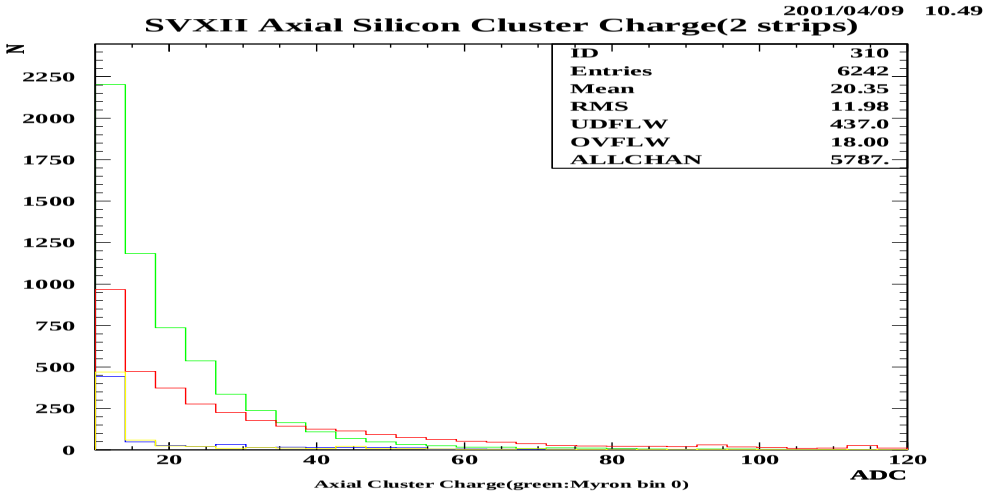




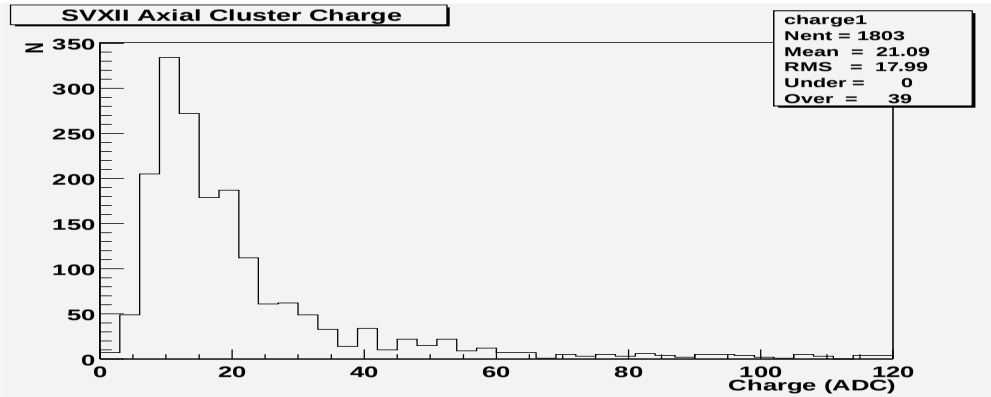
Gross timing in

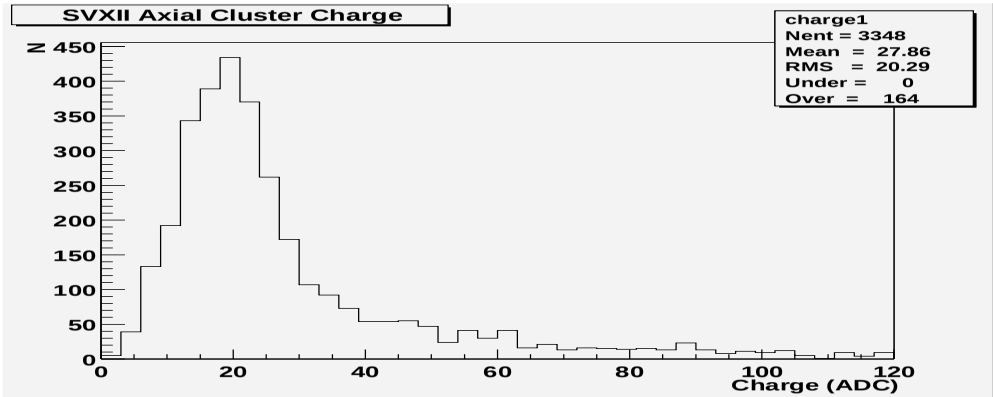
For each L1A, tag 4 different cells. Look at charge clusters in each bucket



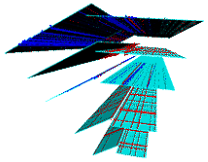


Using hits on track look at Landau distributions as you scan within 132 ns:





DAQ Status



CDF has been collecting DATA with 70% of SVXII 40 % of ISL fully integrated since late July 2001. Accelerator operating with 396ns bunch crossing time and 36x36 bunches. CDF DAQ operating using 132ns clocks.

- *All wedges are plugged in and have full DAQ instrumentation. 3/72 SVX 1/2 wedges have readout problems - not fully understood.*
- *Problems with TX DOIM light outputs, matching to RX DOIMS are causing high bit error rates. Problems understood and fixable.*
- Ran with L1A rate of up to 4KHz. Firmware upgrades to run at 50KHz being implemented. L3 software trigger operating at spec.
- *SVT finding tracks ! (see Simone's talk).*
- 1st PHYSICS SIGNALS SEEN : $Z \to ee$, $W \to \mu/e\nu$, $J/\psi \to \mu\mu$, $\Lambda \to p\pi$, $K_s \to \pi\pi$, $B^{\pm} \to J/\psi K^{\pm}$,